FIG. 1A

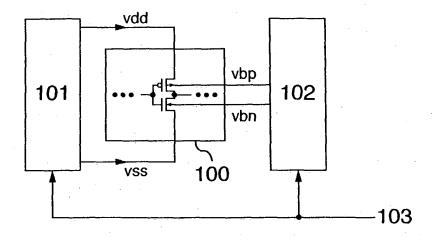


FIG. 1B

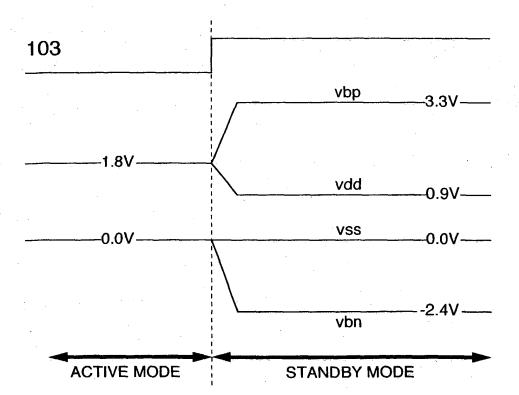


FIG. 2

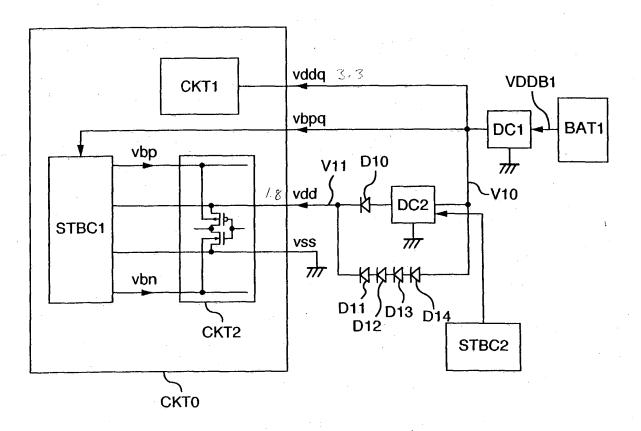


FIG. 4

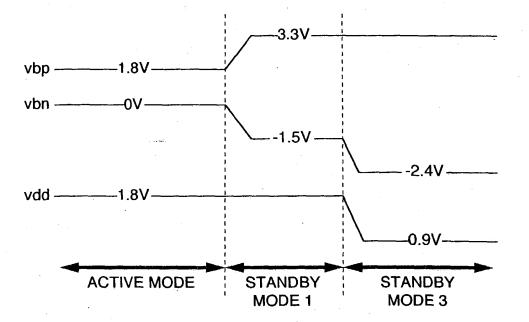


FIG. 5A

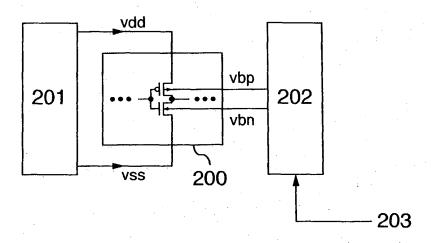


FIG. 5B

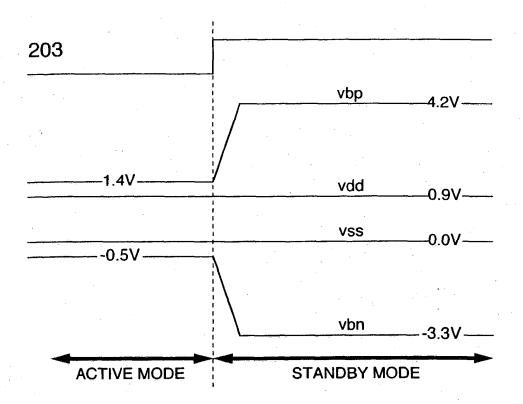


FIG. 6

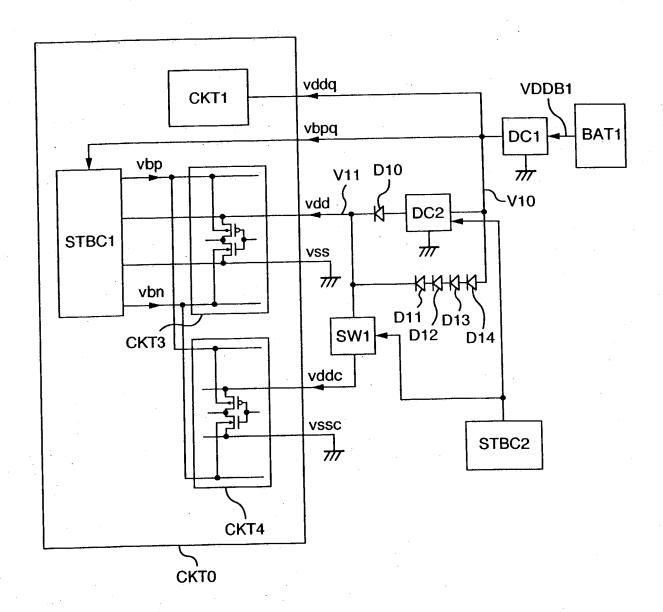


FIG. 7

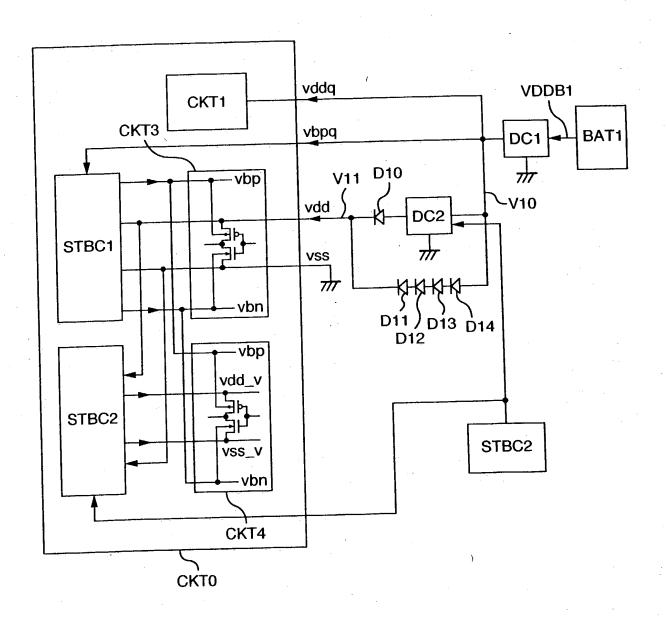


FIG. 8

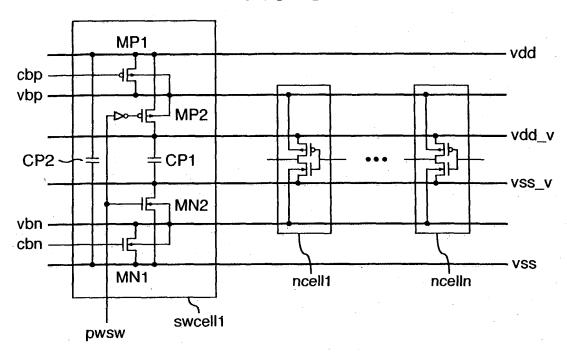


FIG. 9

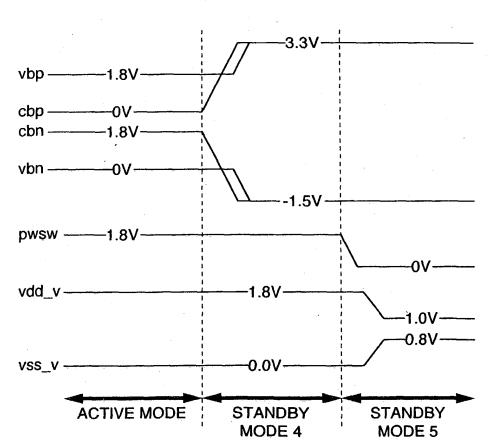
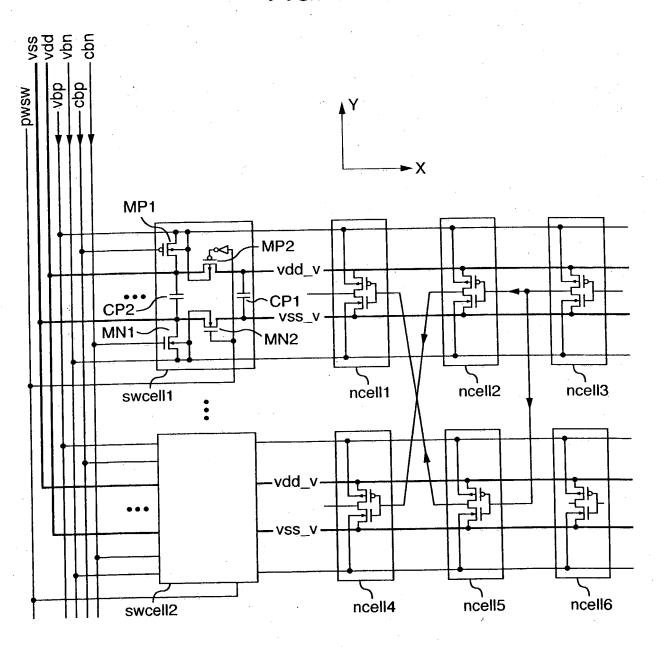


FIG. 10



→ SIGNAL FLOW

FIG. 11

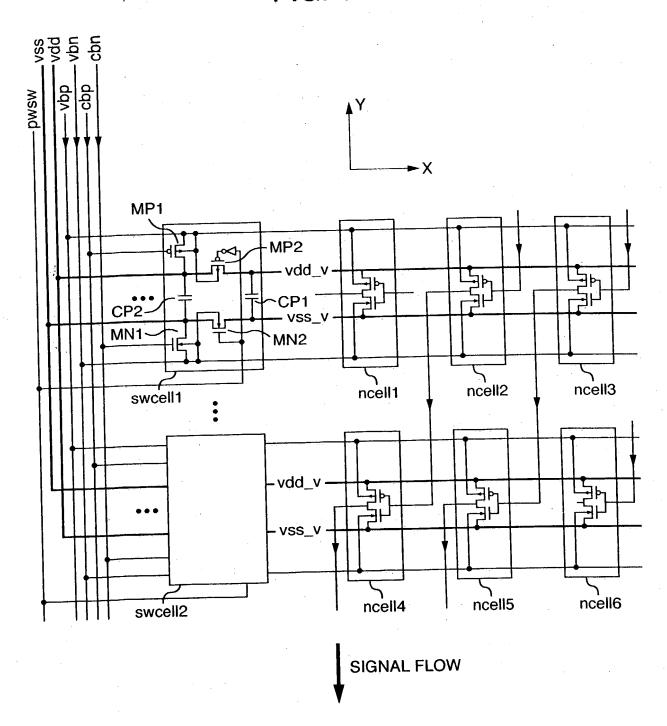


FIG. 12

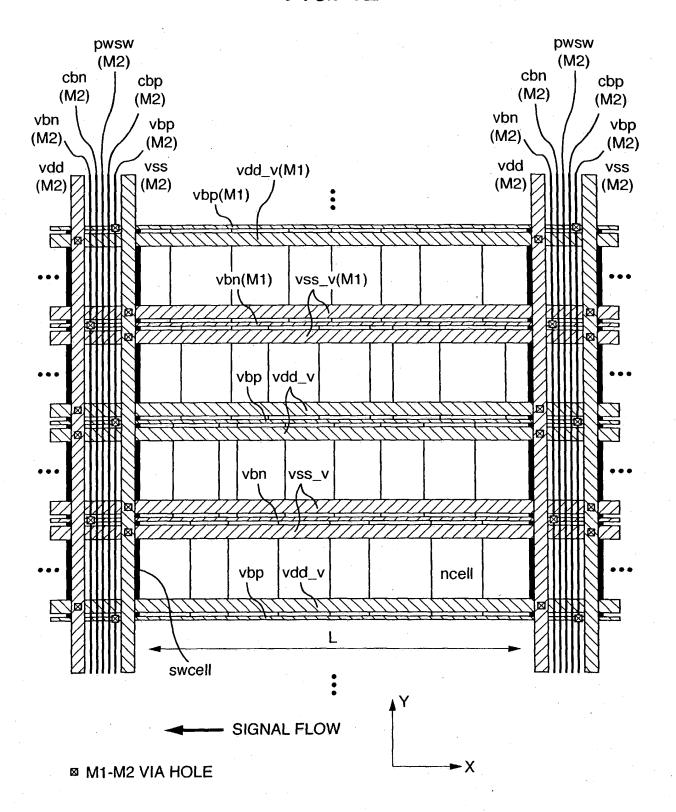


FIG. 13

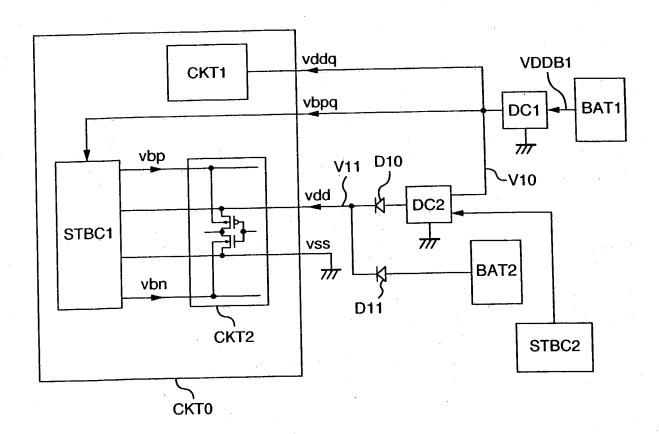


FIG. 14A

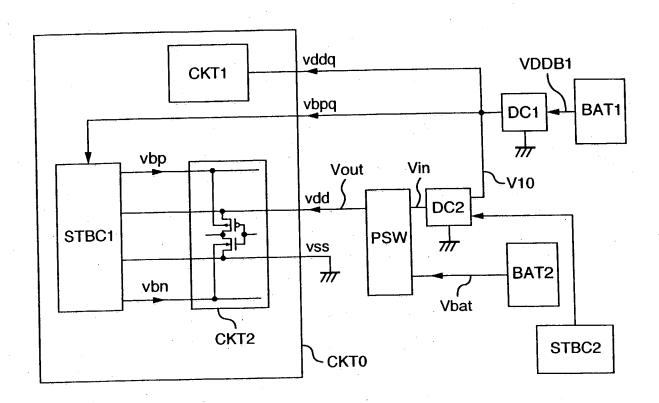


FIG. 14B

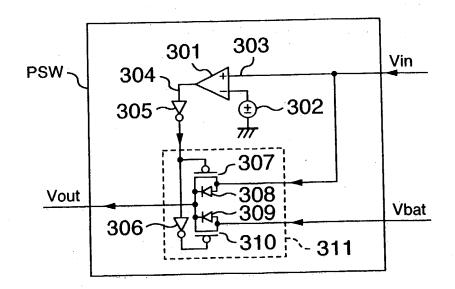


FIG. 15

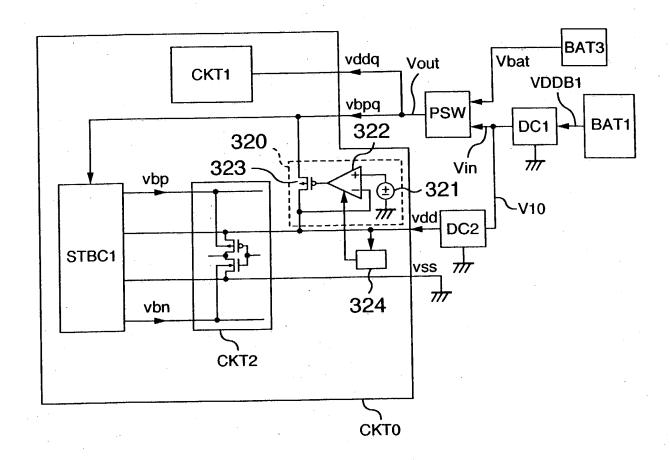


FIG. 16

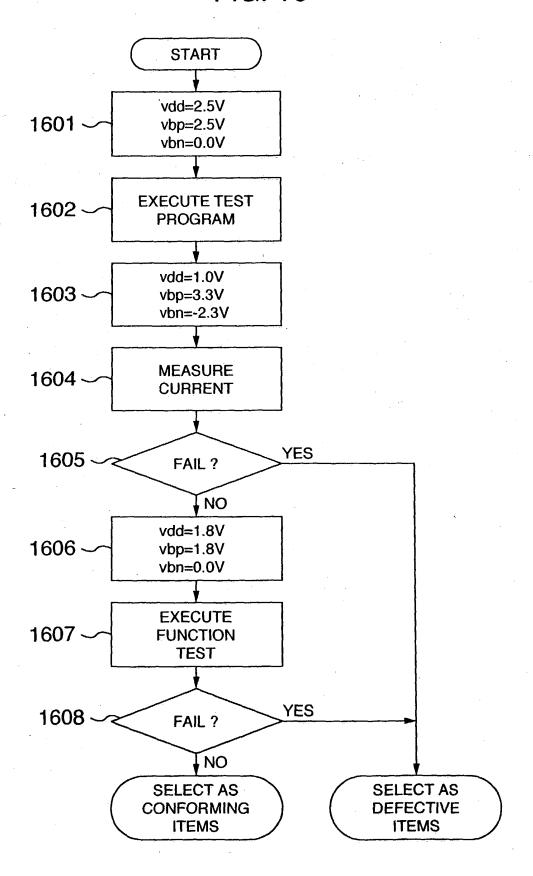


FIG. 17

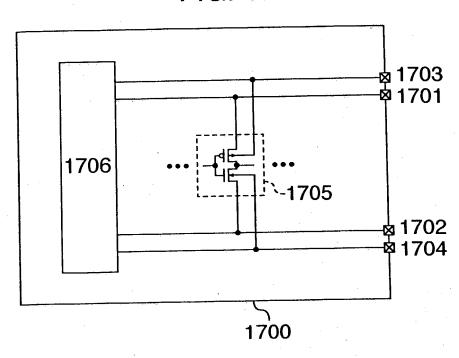


FIG. 18

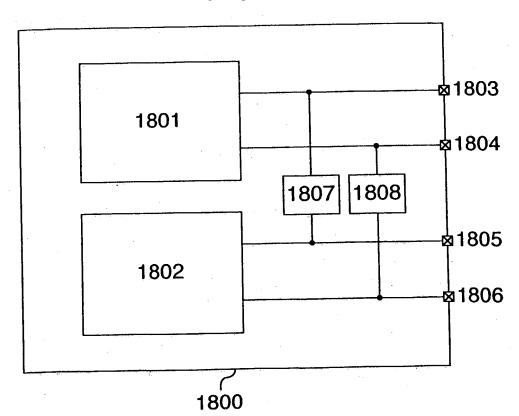
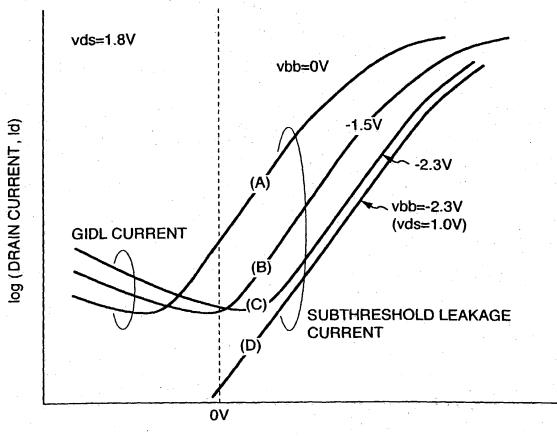


FIG. 19A



GATE VOLTAGE ,Vgs

FIG. 19B

	vds(V)	vbb(V)
( <u>A</u> )	1.8	0
(B)	1.8	-1.5
(C)	1.8	-2.3
(D)	1.0	-2.3